BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants:	**DEISS, Michael Scott, et al.**
Ser. No.:	**09/582,451**
Filed:	**November 10, 2000**
For:	**APPARATUS FOR PROVIDING A VIDEO LIP SYNC DELAY AND METHOD THEREFORE**
Examiner:	**AN, Shawn S.**
Art Unit:	**2621**

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the final Office Action dated December 29, 2009, and further to the Notice of Appeal filed on March 26, 2010, Appellants hereby submit an Appeal Brief in accordance with 37 C.F.R. §41.37 for the above-referenced application.

I. Real Party in Interest

The real party in interest is Thomson Licensing LLC.

II. Related Appeals and Interferences

There are no prior or pending appeals, interferences, or judicial proceedings known to Appellants, the Appellants' legal representative, or assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. Status of Claims

Claims 13-32 are pending in this application, and are rejected. Claims 1-12 are cancelled. The rejection of claims 13-32 is being appealed.

IV. Status of Amendments

No amendment subsequent to the final rejection of December 29, 2009 has been filed.

V. Summary of Claimed Subject Matter

Independent claim 13 defines a receiver (see, for example, element 15 of FIG. 1) comprising:

(a) a first input for receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data (see, for example, inputs to elements 1500 and/or 1501 of FIG. 1 and page 4, line 20 to page 5, line 2);

(b) a second input for receiving an analog signal (see, for example, EXT input to element 1540 of FIG. 1);

(c) a decoder unit partitioning said packetized data stream to generate a video component and an audio component (see, for example, element 1507 of FIG. 1 and page 5, lines 4-10);

(d) a processor processing said analog signal to generate a digitized audio signal and a digitized video signal (see, for example, elements 1540, 1550 and 1560 of FIG. 1);

(e) first digital signal processing arrangement decompressing said video component of said packetized data stream, and digital signal processing said decomposed video component and said digitized video signal to generate a video output signal (see, for example, element 1511 of FIG. 1, page 5, line 26 to page 6, line 11, and page 7, lines 12-23);

(f) second digital signal processing arrangement decompressing said audio component of said packetized data stream, and digital signal processing said decompressed audio component and said digitized audio signal to generate an audio output signal (see, for example, element 1513 of FIGS. 1 and 2, page 6, lines 13-29, page 7, lines 12-23, and page 7, line 25 to page 8, line 28);

(g) a delay selectively delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal (see, for example, element 1607 of FIG. 2 and page 8, lines 17-28); and

(h) a converting arrangement transposing said video output signal to the displayable video signal and said audio output signal to the audible output signal (see, for example, elements 1519, 1523, 1525, 1529 of FIG. 1 and page 6, lines 1-33).

Dependent claim 19 further defines the receiver of claim 13, and states: wherein said first digital signal processing arrangement comprises a converter converting said digitized video signal having an interlace video format into a digitized video signal having a progressive scan format (see, for example, element 1511 of FIG. 1 and page 5, line 26 to page 6, line 11).

Independent claim 20 defines a method for processing input signals having video and audio components (see, for example, page 2, lines 26-29), said method comprising:

receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data

(see, for example, inputs to elements 1500 and/or 1501 of FIG. 1 and page 4, line 20 to page 5, line 2);

receiving an analog signal (see, for example, EXT input to element 1540 of FIG. 1);

partitioning said packetized data stream to generate a video component and an audio component (see, for example, element 1507 of FIG. 1 and page 5, lines 4-10);

processing said analog signal to generate a digitized video signal and a digitized audio signal (see, for example, elements 1540, 1550 and 1560 of FIG. 1);

decompressing said video component of said packetized data stream to generate a decompressed video signal, and digital signal processing said decompressed video signal and said digitized video signal to generate a video output signal (see, for example, element 1511 of FIG. 1, page 5, line 26 to page 6, line 11, and page 7, lines 12-23);

decompressing said audio component of said packetized data stream to generate a decompressed audio signal, and digital signal processing said decompressed audio signal and said digitized audio signal to generate an audio output signal (see, for example, element 1513 of FIGS. 1 and 2, page 6, lines 13-29, page 7, lines 12-23, and page 7, line 25 to page 8, line 28);

delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal (see, for example, element 1607 of FIG. 2 and page 8, lines 17-28); and

transposing said video output signal to the displayable video signal and said audio output signal to the audible output signal (see, for example, elements 1519, 1523, 1525, 1529 of FIG. 1 and page 6, lines 1-33).

Dependent claim 23 further defines the method of claim 20, and states: further comprising converting said digitized video signal into a progressive scan format (see, for example, element 1511 of FIG. 1 and page 5, line 26 to page 6, line 11).

Independent claim 24 defines a receiver (see, for example, element 15 of FIG. 1) comprising:

a tuner receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data (see, for example, elements 1500 and/or 1501 of FIG. 1 and page 4, line 20 to page 5, line 2);

an input for receiving an analog signal (see, for example, EXT input to element 1540 of FIG. 1);

a processor processing said analog signal to generate a digitized audio signal and a digitized video signal (see, for example, elements 1540, 1550 and 1560 of FIG. 1);

a transport decoder unit partitioning said packetized data stream to generate a video component and an audio component (see, for example, element 1507 of FIG. 1 and page 5, lines 4-10);

a first digital signal arrangement decompressing said video component to generate decompressed video signal, wherein said first digital signal processing arrangement applies a first digital signal processing function to said decompressed video signal and said digitized video signal to produce a video output signal (see, for example, element 1511 of FIG. 1, page 5, line 26 to page 6, line 11, and page 7, lines 12-23);

a second digital signal arrangement decompressing said audio component to generate decompressed audio signal, wherein said second digital signal processing arrangement applies a second digital signal processing function to said decompressed audio signal and said digitized audio signal to generate an audio output signal (see, for example, element 1513 of FIGS. 1 and 2, page 6, lines 13-29, page 7, lines 12-23, and page 7, line 25 to page 8, line 28);

a delay selectively delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal (see, for example, element 1607 of FIG. 2 and page 8, lines 17-28); and

a converting arrangement transposing said video output signal to the displayable video signal and said audio output signal to the audible output signal (see, for example, elements 1519, 1523, 1525, 1529 of FIG. 1 and page 6, lines 1-33).

VI. Grounds of Rejection to be Reviewed on Appeal

The following grounds of rejection are presented for review in this appeal:

A. The rejection of claims 13-18, 20-22 and 24-32 under 35 U.S.C. §103(a) based on the proposed combination of U.S. Patent No. 6,134,419 issued to Williams (hereinafter, "Williams"), U.S. Patent No. 5,602,595 issued to Citta et al. (hereinafter, "Citta") and U.S. Patent No. 5,898,695 issued to Fujii et al. (hereinafter, "Fujii"); and

B. The rejection of claims 19 and 23 under 35 U.S.C. §103(a) based on the proposed combination of Williams, Citta, Fujii and U.S. Patent No. 5,963,261 issued to Dean (hereinafter, "Dean").

VII. Argument

A. Patentability of Claims 13-18, 20-22 and 24-32

The rejection of claims 13-18, 20-22 and 24-32 under 35 U.S.C. §103(a) based on the proposed combination of Williams, Citta and Fuji should be reversed for at least the following reasons.

Appellants first note that the present invention relates to a receiver that is adapted to receive both conventional SDTV analog signals and compressed digital signals. As known in the art, and as described in Appellants' specification, SDTV analog signals are not compressed. One of the reasons SDTV analog signals are not compressed is that the SDTV analog signals are not in digital format. Accordingly, one aspect of the present invention is that received SDTV analog signals are digitized, so that digital signal processing resources can be shared by both digitized analog signals and compressed digital signals. For example, element 1511 in FIG. 1 performs both video MPEG decoding and up-converting because element 1511 is a video MPEG decoder and up-converter (see, for example, page 7, lines 18-21). The up-converting function, thus, is shared by both digitized analog video signals and decompressed MPEG video signals. An example of the sharing the audio digital signal processing resources is shown by audio MPEG/AC-3 decoder 1513 of FIG. 2, where the processing functions in the subsequent audio processing block 1609 are shared by both digitized analog audio signals and decompressed MPEG audio signals (see, for

example, page 7, line 36-page 8, line 2). These sharing arrangements of the present invention are particularly advantageous since they can simplify system design and reduce the cost for a receiver capable of receiving both analog signals and compressed digital signals. Appellants have also recognized that an audio output signal corresponding to a digitized audio signal must be selectively delayed in order to synchronize a displayable analog video signal with an audible analog audio signal in this particular environment.

For example, independent claim 13 recites a receiver, comprising:

> (a) a first input for receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data;
> (b) a second input for receiving an analog signal;
> (c) a decoder unit partitioning said packetized data stream to generate a video component and an audio component;
> (d) a processor processing said analog signal to generate a digitized audio signal and a digitized video signal;
> (e) first digital signal processing arrangement decompressing said video component of said packetized data stream, and digital signal processing said decomposed video component and said digitized video signal to generate a video output signal;
> (f) second digital signal processing arrangement decompressing said audio component of said packetized data stream, and digital signal processing said decompressed audio component and said digitized audio signal to generate an audio output signal;
> (g) a delay selectively delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal; and
> (h) a converting arrangement transposing said video output signal to the displayable video signal and said audio output signal to the audible output signal. (emphasis added)

As indicated above, the "digitized audio signal" and "digitized video signal" recited in the claim are digitalized analog audio and video signals because the "processor" processes the "analog signal" to generate the "digitized audio signal" and the "digitized video signal". Moreover, the "analog signal" is not compressed because the "first digital signal processing arrangement" processes the "digitized video signal" to

produce the "video output signal" (without performing a decompressing function on the "digitized video signal"), and the "second digital processing arrangement" processes the "digitized audio signal" to generate the "audio output signal" (without performing a decompressing function on the "digitized audio signal"). That is, according to the claim language, the "first digital signal processing arrangement" and the "second digital signal processing arrangement" only decompress the "video component of said packetized data stream" and the "audio component of said packetized data stream", respectively (both of which are digital signals).

Neither Williams, Citta nor Fujii, whether taken individually or in combination, discloses or suggests, *inter alia*, each and every element of the claimed invention.

First, Appellants submit that none of the cited references discloses a receiver that is adapted to receive both compressed digital signals and analog signals, as claimed. In fact, all three references disclose receivers that receive compressed digital signals. As admitted by the Examiner in the final Office Action of December 29, 2009, Williams discloses a receiver for receiving compressed digital signals. Appellants submit that Citta and Fujii also disclose a receiver receiving compressed digital signals, as discussed below.

Citta discloses a receiver for receiving compressed digital signals because the reference clearly states at column 3, lines 57-67 in describing the receiver shown in FIG. 4 that the received signal is an MPEG signal without the MPEG sync bytes. As such, although an A/D is involved, since the received signal is an MPEG signal, the received signal is a compressed digital signal, not an analog signal, as claimed.

In the final Office Action of December 29, 2009, the Examiner alleges that FIG. 4 of Citta discloses an ATV receiver/sync system comprising an input for receiving an analog signal. Appellants respectfully disagree. As discussed above, FIG. 4 of Citta clearly shows that the receiver receives an MPEG signal as clearly evident by the presence of an MPEG sync reinsertion block 40 in processing the input signal. As is well known in the art, in order to transmit an MPEG signal, for example, in the air, bits

may be added to the MPEG signal for error correction and detection. The MPEG signal is then modulated and RF transmitted. On the receiver side, a receiver must demodulate and remove the added bits to recover the MPEG signal. The fact that a receiver, such as the one disclosed by Citta, digitizes the RF signal using an A/D to recover the MPEG signal is irrelevant to independent claim 13 because claim 13 does not recite how the compressed digital signal is recovered in a receiver. Furthermore, although MPEG signals are RF transmitted, it does not convert MPEG signals into analog signals under the meaning of claim 13. For example, the MPEG signals received in the receiver disclosed in the present application are also RF transmitted, but they are compressed digital signals (s ee, for example, page 4, lines 1-34, of the specification of the present application). Accordingly, Appellants submit that Citta discloses a receiver for receiving compressed digital signals, not an "analog signal" in the manner claimed.

Fujii also discloses a receiver for receiving compressed video signals. For example, at column 3, lines 60-64, Fujii states that the object of the invention is to provide a decoder for compressed and multiplexed video and audio data, wherein packet landing buffers are allocated in a RAM used by a CPU for the system control to hereby reduce the number of components and lower the cost of component. In fact, the phrases "MPEG" and "MPEG transport packets" are used throughout the specification.

Accordingly, for at least the foregoing reasons, Appellants submit that none of the cited references, whether taken individually or in combination, discloses a receiver that is adapted to receive both compressed digital signals and analog signals, as claimed.

Also in the final Office Action of December 29, 2009, the Examiner alleges that Williams discloses the claimed "first digital signal processing arrangement" and "second digital signal processing arrangement" of independent claim 13. Specifically, the Examiner alleges that the claimed "first digital signal processing arrangement" is disclosed by element 122 of FIGS. 7 and 8, and that the claimed "second digital signal

processing arrangement" is disclosed by element 123 of FIGS. 7 and 8. Appellants respectfully disagree for at least the following reasons.

As indicated above, the claimed "first digital signal processing arrangement" and "second digital signal processing arrangement" each processes two different types of signals, namely a decompressed digital signal and a digitized analog signal, in order to generate an output signal. Williams nowhere discloses or suggests that elements 122 or 123 (i.e., the alleged "first digital signal processing arrangement" and "second digital signal processing arrangement") process these two different types of signals (see FIGS. 7 and 8). Rather, elements 122 and 123 each process only a decompressed digital signal. Accordingly, the proposed combination including the teachings of Williams fails to disclose or suggest, *inter alia*, the claimed "first digital signal processing arrangement" and "second digital signal processing arrangement" which, as indicated above, are advantageous sharing arrangements which can simplify system design and reduce the cost for a receiver capable of receiving both analog signals and compressed digital signals.

Furthermore, the final Office Action of December 29, 2009 cites Fujii as disclosing a delay means for selectively delaying the processing of the digitized audio signal to synchronize an audible audio signal with the displayable video signal. However, since Fujii does not disclose or suggest a receiver receiving an analog signal, there is no digitized analog signal in the receiver. As such, Fujii does not disclose the delay element of claim 13.

Accordingly, as discussed above, since none of the three cited references discloses or suggests receiving an "analog signal", the three cited references, considered individually or in combination, do not disclose or suggest "a second input for receiving an analog signal", "a processor processing the analog signal to generate a digitized audio signal and a digitized video signal", the "first digital signal processing arrangement decompressing the video component of the packetized data stream, and digital signal processing the decomposed video component and the digitized video signal to generate a video output", the "second digital signal processing arrangement

decompressing the audio component of the packetized data stream, and digital signal processing the decompressed audio component and the digitized audio signal to generate an audio output signal", and "a delay selectively delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal", as recited by independent claim 13. As such, Appellants submit that independent claim 13 and its respective dependent claims are patentable over the proposed combination of Williams, Citta and Fujii. Moreover, since independent claims 20 and 24 recite features similar to that of independent claim 13, Appellants further submit that independent claims 20 and 24 and their respective dependent claims are also patentable over the proposed combination of Williams, Citta and Fujii.

For at least the foregoing reasons, Appellants respectfully request that the Board reverse the rejection of claims 13-18, 20-22 and 24-32.

B. Patentability of Claims 19 and 23

The rejection of claims 19 and 23 under 35 U.S.C. §103(a) based on the proposed combination of Williams, Citta, Fuji and Dean should be reversed for at least the following reasons. Dean discloses a low cost scan converter, but does not disclose a receiver, as claimed. Since Dean does not disclose a receiver, it fails to cure the defects of Williams, Fujii, and Citta as applied to independent claims 13 and 20 (from which claims 19 and 23 depend). Accordingly, Appellants respectfully request that the Board reverse the rejection of claims 19 and 23.

VIII. Claims Appendix

13. A receiver comprising:

(a) a first input for receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data;

(b) a second input for receiving an analog signal;

(c) a decoder unit partitioning said packetized data stream to generate a video component and an audio component;

(d) a processor processing said analog signal to generate a digitized audio signal and a digitized video signal;

(e) first digital signal processing arrangement decompressing said video component of said packetized data stream, and digital signal processing said decomposed video component and said digitized video signal to generate a video output signal;

(f) second digital signal processing arrangement decompressing said audio component of said packetized data stream, and digital signal processing said decompressed audio component and said digitized audio signal to generate an audio output signal;

(g) a delay selectively delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal; and

(h) a converting arrangement transposing said video output signal to the displayable video signal and said audio output signal to the audible output signal.

14. The receiver of claim 13 wherein said delay comprises an adjustable memory device.

15. The receiver of claim 14 wherein said delay is connected to said second digital signal processing arrangement.

16. The receiver of claim 13 wherein said delay includes said partitioning decoder unit.

17. The receiver of claim 13 wherein said second digital signal processing arrangement further comprises a processing element digital signal processing the digitized audio signal and the decompressed audio component.

18. The receiver of claim 17 wherein said processing element in said second digital signal processing arrangement comprises a surround sound processor.

19. The receiver of claim 13 wherein said first digital signal processing arrangement comprises a converter converting said digitized video signal having an interlace video format into a digitized video signal having a progressive scan format.

20. A method for processing input signals having video and audio components, said method comprising:

receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data;

receiving an analog signal;

partitioning said packetized data stream to generate a video component and an audio component;

processing said analog signal to generate a digitized video signal and a digitized audio signal;

decompressing said video component of said packetized data stream to generate a decompressed video signal, and digital signal processing said decompressed video signal and said digitized video signal to generate a video output signal;

decompressing said audio component of said packetized data stream to generate a decompressed audio signal, and digital signal processing said decompressed audio signal and said digitized audio signal to generate an audio output signal;

delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal; and

transposing said video output signal to the displayable video signal and said audio output signal to the audible output signal.

21. The method of claim 20 wherein the step of delaying is performed before the step of digital signal processing said digitized audio signal has been completed.

22. The method of claim 21 wherein the step of delaying is performed before the step of digital signal processing said digitized audio signal.

23. The method of claim 20 further comprising converting said digitized video signal into a progressive scan format.

24. A receiver comprising:

a tuner receiving a packetized input data stream comprised of multiplexed and compressed packets, each of said packets having at least header and payload data;

an input for receiving an analog signal;

a processor processing said analog signal to generate a digitized audio signal and a digitized video signal;

a transport decoder unit partitioning said packetized data stream to generate a video component and an audio component;

a first digital signal arrangement decompressing said video component to generate decompressed video signal, wherein said first digital signal processing arrangement applies a first digital signal processing function to said decompressed video signal and said digitized video signal to produce a video output signal;

a second digital signal arrangement decompressing said audio component to generate decompressed audio signal, wherein said second digital signal processing arrangement applies a second digital signal processing function to said decompressed audio signal and said digitized audio signal to generate an audio output signal;

a delay selectively delaying the audio output signal for the digitized audio signal to synchronize an audible audio signal with a displayable video signal; and

a converting arrangement transposing said video output signal to the displayable video signal and said audio output signal to the audible output signal.

25. The receiver of claim 24, wherein the delay is disposed such that the delaying occurs before the digital signal processing of the digitized audio signal has been completed.

26. The receiver of claim 25, wherein the delaying occurs before the digital signal processing of the digitized audio signal.

27. The receiver of claim 24, wherein the delay is disposed such that the delaying occurs after the digital signal processing of the digitized audio signal.

28. The receiver of claim 13, wherein the delay is disposed such that the delaying occurs before the digital signal processing of the digitized audio signal has been completed.

29. The receiver of claim 28, wherein the delaying occurs before the digital signal processing of the digitized audio signal.

30. The receiver of claim 13, wherein the delay is disposed such that the delaying occurs after the digital signal processing of the digitized audio signal.

31. The receiver of claim 13, wherein the first digital signal processing arrangement comprises a converting element for digital signal processing the digitized video signal and the decompressed video component.

32. The method of claim 20 wherein the step of delaying is performed after the step of digital signal processing said digitized audio signal.

IX. Evidence Appendix

None.

X. Related Proceedings Appendix

None.

Please charge the fee for this Appeal Brief to Deposit Account 07-0832.

Respectfully submitted,

/Reitseng Lin/

By: Reitseng Lin
Reg. No. 42,804
Phone (609) 734-6813

Patent Operations
Thomson Licensing LLC
P.O. Box 5312
Princeton, New Jersey 08540
May 10, 2010